







Design Rules Verification Report

Filename : D:\Users\RadiganConagher\Documents\circuits\pps_piggy\board.PcbDoc

Warnings 0
Rule Violations 2

Warnings	
Total	0

Rule Violations	
Short-Circuit Constraint (Allowed=Yes) (InNet('RX')),(InNet('RX_AB'))	0
Clearance Constraint (Gap=23.622mil) (InPolygon),(InComponentClass('FarFill'))	0
Clearance Constraint (Gap=8mil) (All),(All)	0
Width Constraint (Min=8mil) (Max=12mil) (Preferred=8mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint (All)	0
Minimum Annular Ring (Minimum=7mil) (All)	0
Hole Size Constraint (Min=13mil) (Max=250mil) (All)	0
Height Constraint (Min=0mil) (Max=10000mil) (Preferred=500mil) (All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0mil) (All),(All)	0
Silkscreen Over Component Pads (Clearance=1mil) (All),(All)	0
Silk to Silk (Clearance=1mil) (All),(All)	2
Net Antennae (Tolerance=0mil) (All)	0
Short-Circuit Constraint (Allowed=Yes) (InNet('+5')),(InNet('VANT'))	0
Net Antennae (Tolerance=1000mil) (InNet('VANT') or InNet('RX'))	0
Total	2

Silk to Silk (Clearance=1mil) (All),(All)	
Text "PPS Out" (-698.819mil,285.433mil) Top Overlay	Arc (-492.126mil,320.866mil) Top Overlay
Text "open source" (-1295.906mil,381.024mil) Bottom Overlay	Text "hardware" (-1335.906mil,331.024mil) Bottom Overlay

Electrical Rules Check Report

Class	Document	Message
Warning	main.SchDoc	Net NetP2_6 has no driving source (Pin P2-6,Pin R3-1)
Warning	main.SchDoc	Net NetP2_8 has no driving source (Pin P2-8,Pin R4-1)
Warning	main.SchDoc	Net RX has no driving source (Pin J2-2,Pin P1-5)
Warning	main.SchDoc	Net USBCFG has no driving source (Pin D1-2,Pin U2-6,Pin U4-15)