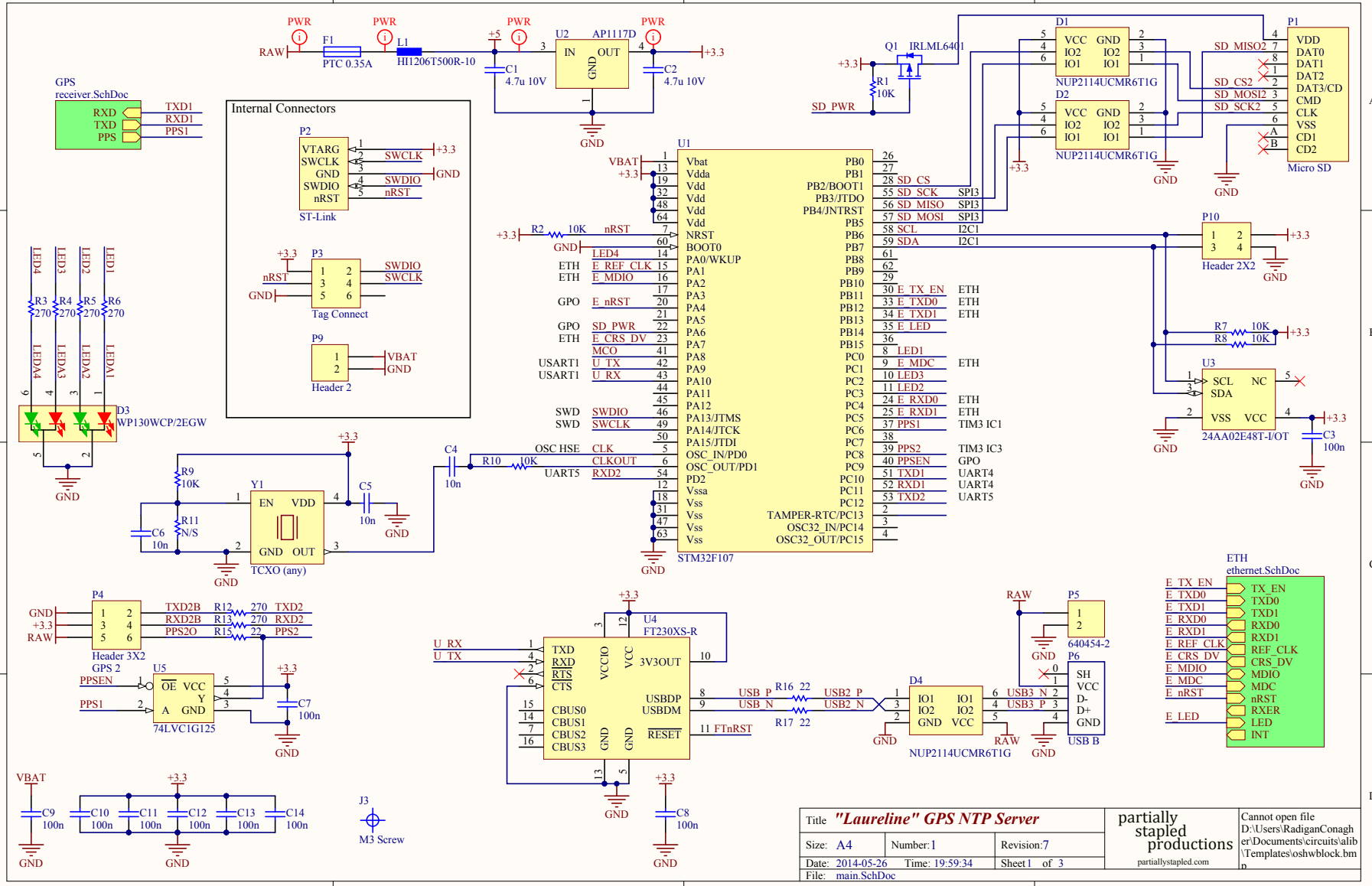
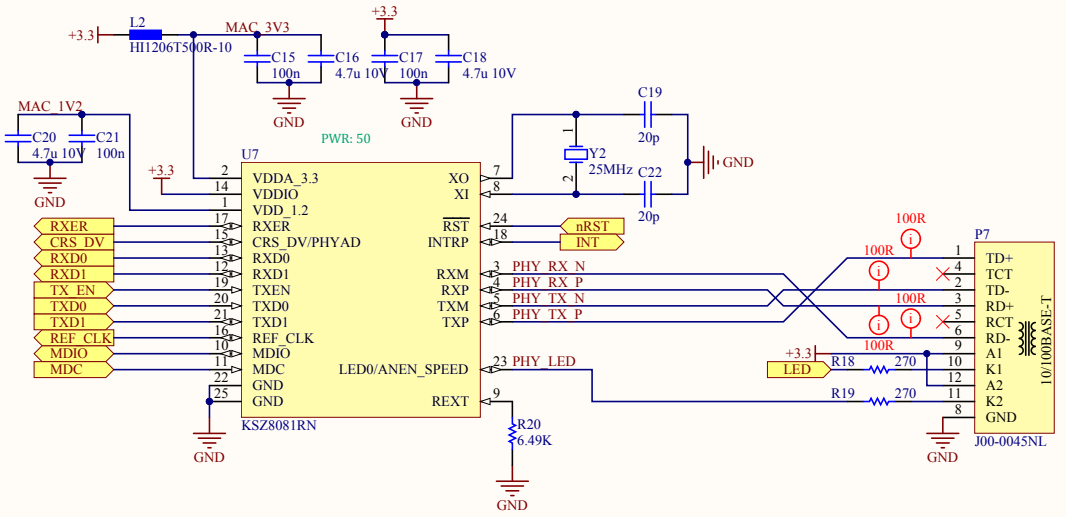
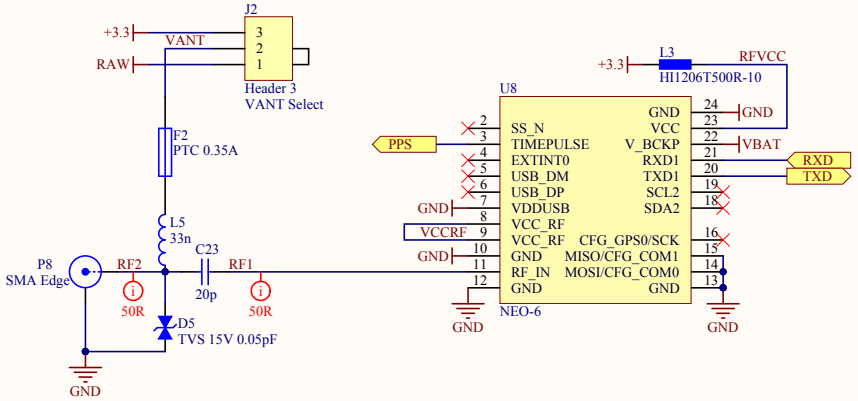

GPS
receiver.SchDoc
RXD
TXD
PPS
TXD1
RXD1
PPS1
Internal Connectors
P2
VTARG
SWCLK
GND
SWDIO
nRST
ST-Link
P3
Tag Connect
P9
Header 2
PWR
RAW
F1
PTC 0.35A
L1
HI1206T500R-10
+5
C1
4.7u 10V
U2
AP1117D
IN
OUT
GND
+3.3
C2
4.7u 10V
Q1
IRLML6401
R1
10K
SD_PWR
D1
NUP2114UCMR6T1G
D2
NUP2114UCMR6T1G
P1
Micro SD
SD_MISO2
SD_CS2
SD_MOSI2
SD_SCK2
VDD
DAT0
DAT1
DAT2
DAT3/CD
CMD
CLK
VSS
CD1
CD2
U1
STM32F107
VBAT
Vbat
Vdda
Vdd
Vss
NRST
BOOT0
PA0/WKUP
PB0
PB1
PB2/BOOT1
PB3/JTDO
PB4/JNTRST
PB5
PB6
PB7
PB8
PB9
PB10
PB11
PB12
PB13
PB14
PB15
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
PC8
PC9
PC10
PC11
PC12
TAMPER-RTC/PC13
OSC32_IN/PC14
OSC32_OUT/PC15
SD_CS
SD_SCK
SD_MISO
SD_MOSI
SCL
SDA
E_TX_EN
E_TXD0
E_TXD1
E_LED
E_MDIO
E_RXD0
E_RXD1
E_REF_CLK
E_CRS_DV
MCO
U_TX
U_RX
SWDIO
SWCLK
OSC_IN/PD0
OSC_OUT/PD1
PD2
Vssa
LED4
E_nRST
SD_PWR
LED3
LED2
E_RXD0
E_RXD1
PPS1
TIM3 IC1
TIM3 IC3
PPSEN
TXD1
RXD1
TXD2
RXD2
CLK
CLKOUT
OSC HSE
UART5
R2 10K
R10 10K
P10
Header 2X2
R7 10K
R8 10K
U3
24AA02E48T-I/OT
C3 100n
LED4
LED3
LED2
LED1
R3 270
R4 270
R5 270
R6 270
LEDA4
LEDA3
LEDA2
LEDA1
D3
WP130WCP/2EGW
R9 10K
R11 N/S
Y1
TCXO (any)
C4 10n
C5 10n
C6 10n
P4
Header 3X2
TXD2B
RXD2B
PPS2O
R12 270
R13 270
R15 22
TXD2
RXD2
PPS2
GPS 2
U5
74LVC1G125
OE
VCC
A
GND
Y
PPSEN
PPS1
C7 100n
U4
FT230XS-R
TXD
RXD
RTS
CTS
VCCIO
VCC
3V3OUT
USBDP
USBDM
RESET
CBUS0
CBUS1
CBUS2
CBUS3
U_RX
U_TX
USB_P
USB_N
R16 22
R17 22
USB2_P
USB2_N
11 FTnRST
C8 100n
D4
NUP2114UCMR6T1G
P5
640454-2
P6
USB B
SH
VCC
D-
D+
GND
USB3_N
USB3_P
ETH
ethernet.SchDoc
TX_EN
TXD0
TXD1
RXD0
RXD1
REF_CLK
CRS_DV
MDIO
MDC
nRST
RXER
LED
INT
C9 100n
C10 100n
C11 100n
C12 100n
C13 100n
C14 100n
J3
M3 Screw
Title "Laureline" GPS NTP Server
Size: A4
Number: 1
Revision: 7
Date: 2014-05-26
Time: 19:59:34
Sheet 1 of 3
File: main.SchDoc
partially stapled productions
partiallystapled.com
Cannot open file D:\Users\RadiganConagher\Documents\circuits\alib\Templates\oshwblock.bmp



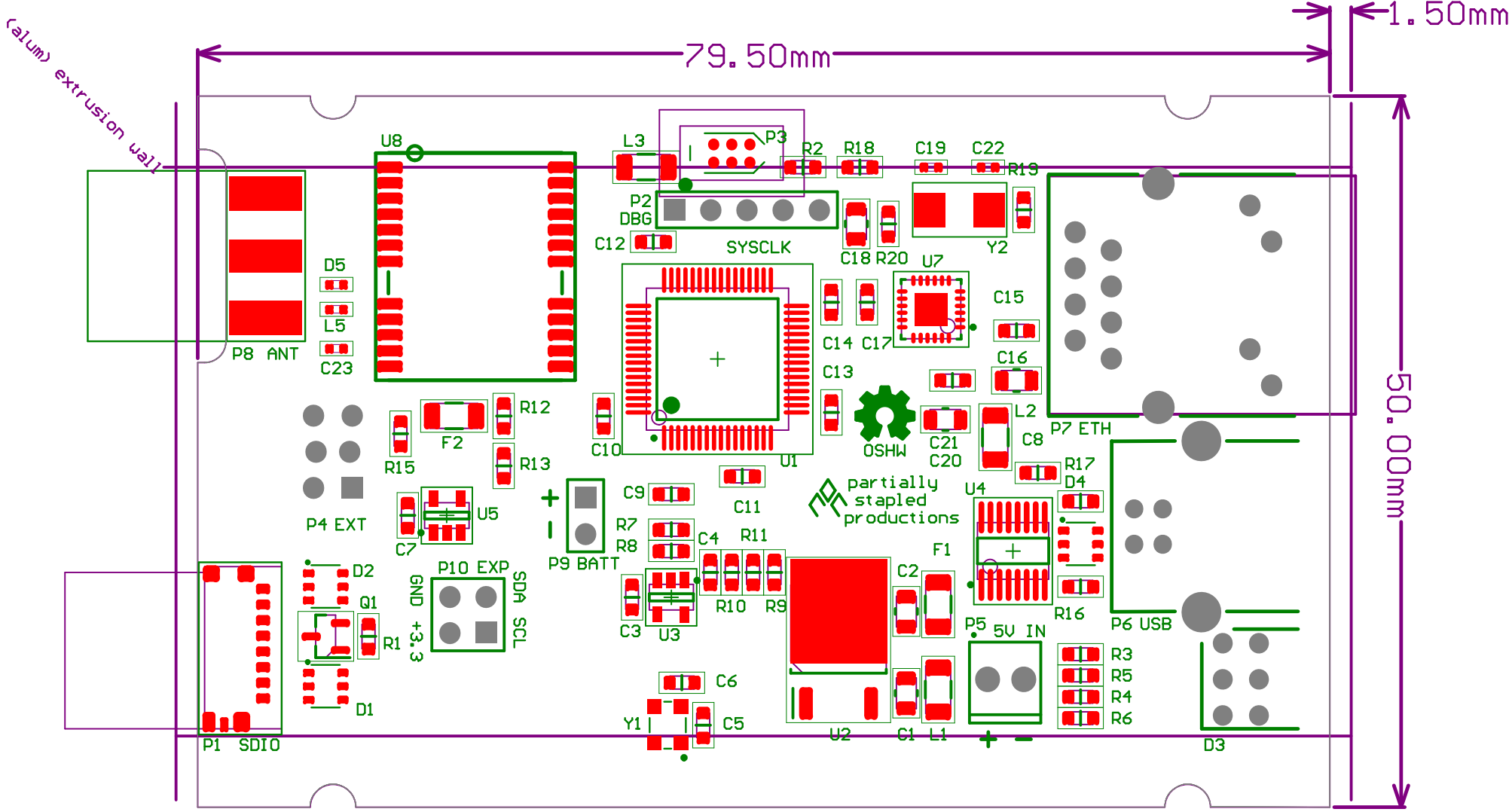

| | | | |
|---|---|---|---|
| Title | *"Laureline" GPS NTP Server* | | |
| Size: A4 | Number: 1 | Revision: 7 | |
| Date: 2014-05-26 | Time: 19:59:34 | Sheet 2 of 3 | |
| File: ethernet.SchDoc | | | |

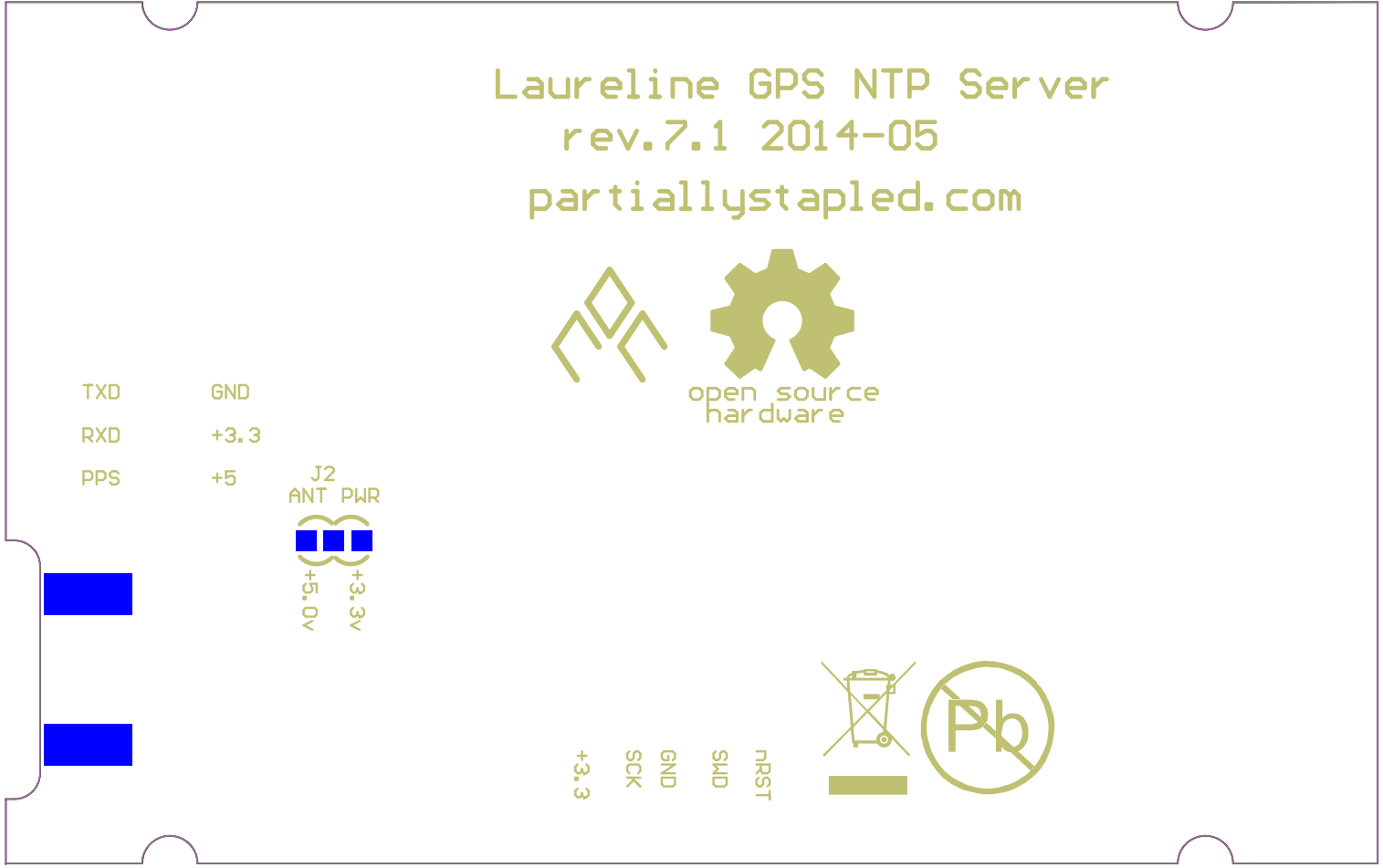
partially stapled productions
partiallystapled.com

Cannot open file D:\Users\RadiganConagher\Documents\circuits\alib\Templates\oshwblock.bmp




| | | | | |
|---|---|---|---|---|
| Title | *"Laureline" GPS NTP Server* | | partially stapled productions | Cannot open file D:\Users\RadiganConagher\Documents\circuits\alib\Templates\oshwblock.bmp |
| Size: A4 | Number: 1 | Revision: 7 | | |
| Date: 2014-05-26 | Time: 19:59:34 | Sheet 3 of 3 | partiallystapled.com | |
| File: receiver.SchDoc | | | | |


(alum) extrusion wall
79.50mm
1.50mm
50.00mm
U8
L3
P3
R2
R18
C19
C22
R19
P2
DBG
SYSCLK
C12
C18
R20
U7
Y2
C15
C14
C17
C16
C13
L2
C8
R17
D4
D5
L5
C23
P8 ANT
R12
F2
R13
R15
C10
U1
OSHW
C21
C20
P7 ETH
P4 EXT
U5
C7
C9
C11
R7
R8
C4
R11
P9 BATT
partially
stapled
productions
U4
F1
C2
P10 EXP
GND
+3.3
SDA
SCL
D2
Q1
R1
D1
C3
U3
R10
R9
R16
P6 USB
P5 5V IN
R3
R5
R4
R6
C6
Y1
C5
U2
C1
L1
P1 SDIO
D3


Laureline GPS NTP Server
rev.7.1 2014-05
partiallystapled.com
open source hardware
TXD
RXD
PPS
GND
+3.3
+5
J2
ANT PWR
+5.0V
+3.3V
+3.3
SCK
GND
SWD
nRST
Pb

# Design Rules Verification Report

Filename : D:\AD10\projects\laureline\hw\board.PcbDoc

Warnings 0
Rule Violations 0

| Warnings | |
|---|---|
| Total | 0 |

| Rule Violations | |
|---|---|
| Width Constraint (Min=0.152mm) (Max=0.203mm) (Preferred=0.203mm) (InNet('GND')) | 0 |
| Net Antennae (Tolerance=25.4mm) (InNet('VANT')) | 0 |
| Clearance Constraint (Gap=0.457mm) ((InDifferentialPairClass('All Differential Pairs') OR | 0 |
| Short-Circuit Constraint (Allowed=Yes) (InNet('RAW')),(InNet('VANT')) | 0 |
| Minimum Annular Ring (Minimum=0.178mm) (All) | 0 |
| Net Antennae (Tolerance=0mm) (All) | 0 |
| Silk to Silk (Clearance=0mm) (All),(All) | 0 |
| Silk To Solder Mask (Clearance=0mm) (IsPad),(All) | 0 |
| Minimum Solder Mask Sliver (Gap=0.076mm) (All),(All) | 0 |
| Hole To Hole Clearance (Gap=0.254mm) (All),(All) | 0 |
| Hole Size Constraint (Min=0.025mm) (Max=10mm) (All) | 0 |
| Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All) | 0 |
| Width Constraint (Min=0.203mm) (Max=0.203mm) (Preferred=0.203mm) (All) | 0 |
| Power Plane Connect Rule(Relief Connect )(Expansion=0.508mm) (Conductor Width=0.254mm) | 0 |
| Un-Routed Net Constraint ( (All) ) | 0 |
| Short-Circuit Constraint (Allowed=No) (All),(All) | 0 |
| Clearance Constraint (Gap=0.254mm) (OnLayer('MidTop') or OnLayer('MidBot')),(All) | 0 |
| Clearance Constraint (Gap=0.6mm) (InPolygon),(IsPad and OnMultiLayer and | 0 |
| Width Constraint (Min=0.328mm) (Max=0.328mm) (Preferred=0.328mm) (InNetClass('50R')) | 0 |
| Clearance Constraint (Gap=0.152mm) (All),(All) | 0 |
| Clearance Constraint (Gap=0.203mm) (Not IsPad),(Not InComponent('U7')) | 0 |
| Width Constraint (Min=0.203mm) (Max=0.406mm) (Preferred=0.203mm) (InNetClass('PWR')) | 0 |
| Total | 0 |

# Electrical Rules Check Report

| Class | Document | Message |
|---|---|---|
| Warning | main.SchDoc | Net E_MDC has no driving source (Pin U1-9,Pin U7-11) |
| Warning | main.SchDoc | Net E_NRST has no driving source (Pin U1-20,Pin U7-24) |
| Warning | ethernet.SchDoc | Net E_TX_EN has no driving source (Pin U1-30,Pin U7-19) |
| Warning | ethernet.SchDoc | Net E_TXD0 has no driving source (Pin U1-33,Pin U7-20) |
| Warning | ethernet.SchDoc | Net NetC22_1 has no driving source (Pin C22-1,Pin U7-8,Pin Y2-2) |
| Warning | ethernet.SchDoc | Net NetR20_2 has no driving source (Pin R20-2,Pin U7-9) |
| Warning | main.SchDoc | Net NRST has no driving source (Pin P2-5,Pin P3-3,Pin R2-2,Pin U1-7) |
| Warning | main.SchDoc | Net PPS1 has no driving source (Pin U1-37,Pin U5-2,Pin U8-3) |
| Warning | main.SchDoc | Net PPSEN has no driving source (Pin U1-40,Pin U5-1) |
| Warning | main.SchDoc | Net SCL has no driving source (Pin P10-1,Pin R7-1,Pin U1-58,Pin U3-1) |
| Warning | main.SchDoc | Nets Wire E_CRS_DV has multiple names (Net Label E_CRS_DV,Net Label E_CRS_DV,Sheet Entry ETH-CRS_DV(Output)) |
| Warning | main.SchDoc | Nets Wire E_CRS_DV has multiple names (Sheet Entry ETH-CRS_DV(Output),Net Label E_CRS_DV,Net Label E_CRS_DV) |
| Warning | main.SchDoc | Nets Wire E_LED has multiple names (Net Label E_LED,Net Label E_LED,Sheet Entry ETH-LED(Input)) |
| Warning | main.SchDoc | Nets Wire E_LED has multiple names (Sheet Entry ETH-LED(Input),Net Label E_LED,Net Label E_LED) |
| Warning | main.SchDoc | Nets Wire E_MDC has multiple names (Net Label E_MDC,Net Label E_MDC,Sheet Entry ETH-MDC(Input)) |
| Warning | main.SchDoc | Nets Wire E_MDC has multiple names (Sheet Entry ETH-MDC(Input),Net Label E_MDC,Net Label E_MDC) |
| Warning | main.SchDoc | Nets Wire E_MDIO has multiple names (Net Label E_MDIO,Net Label E_MDIO,Sheet Entry ETH-MDIO(I/O)) |
| Warning | main.SchDoc | Nets Wire E_MDIO has multiple names (Sheet Entry ETH-MDIO(I/O),Net Label E_MDIO,Net Label E_MDIO) |
| Warning | main.SchDoc | Nets Wire E_NRST has multiple names (Net Label E_NRST,Net Label E_NRST,Sheet Entry ETH-NRST(Input)) |
| Warning | main.SchDoc | Nets Wire E_NRST has multiple names (Sheet Entry ETH-NRST(Input),Net Label E_NRST,Net Label E_NRST) |
| Warning | main.SchDoc | Nets Wire E_REF_CLK has multiple names (Net Label E_REF_CLK,Net Label E_REF_CLK,Sheet Entry ETH-REF_CLK(Output)) |
| Warning | main.SchDoc | Nets Wire E_REF_CLK has multiple names (Sheet Entry ETH-REF_CLK(Output),Net Label E_REF_CLK,Net Label E_REF_CLK) |
| Warning | main.SchDoc | Nets Wire E_RXD0 has multiple names (Net Label E_RXD0,Net Label E_RXD0,Sheet Entry ETH-RXD0(Output)) |
| Warning | main.SchDoc | Nets Wire E_RXD0 has multiple names (Sheet Entry ETH-RXD0(Output),Net Label E_RXD0,Net Label E_RXD0) |
| Warning | main.SchDoc | Nets Wire E_RXD1 has multiple names (Net Label E_RXD1,Net Label E_RXD1,Sheet Entry ETH-RXD1(Output)) |
| Warning | main.SchDoc | Nets Wire E_RXD1 has multiple names (Sheet Entry ETH-RXD1(Output),Net Label E_RXD1,Net Label E_RXD1) |
| Warning | main.SchDoc | Nets Wire E_TX_EN has multiple names (Net Label E_TX_EN,Net Label E_TX_EN,Sheet Entry ETH-TX_EN(Input)) |
| Warning | main.SchDoc | Nets Wire E_TX_EN has multiple names (Sheet Entry ETH-TX_EN(Input),Net Label E_TX_EN,Net Label E_TX_EN) |
| Warning | main.SchDoc | Nets Wire E_TXD0 has multiple names (Net Label E_TXD0,Net Label E_TXD0,Sheet Entry ETH-TXD0(Input)) |
| Warning | main.SchDoc | Nets Wire E_TXD0 has multiple names (Sheet Entry ETH-TXD0(Input),Net Label E_TXD0,Net Label E_TXD0) |
| Warning | main.SchDoc | Nets Wire E_TXD1 has multiple names (Net Label E_TXD1,Net Label E_TXD1,Sheet Entry ETH-TXD1(Input)) |
| Warning | main.SchDoc | Nets Wire E_TXD1 has multiple names (Sheet Entry ETH-TXD1(Input),Net Label E_TXD1,Net Label E_TXD1) |
| Warning | main.SchDoc | Nets Wire PPS1 has multiple names (Net Label PPS1,Net Label PPS1,Net Label PPS1,Sheet Entry GPS-PPS(Output)) |
| Warning | main.SchDoc | Nets Wire PPS1 has multiple names (Sheet Entry GPS-PPS(Output),Net Label PPS1,Net Label PPS1,Net Label PPS1) |
| Warning | main.SchDoc | Nets Wire RXD1 has multiple names (Net Label RXD1,Net Label RXD1,Sheet Entry GPS-TXD(Output)) |
| Warning | main.SchDoc | Nets Wire RXD1 has multiple names (Sheet Entry GPS-TXD(Output),Net Label RXD1,Net Label RXD1) |
| Warning | main.SchDoc | Nets Wire TXD1 has multiple names (Net Label TXD1,Net Label TXD1,Sheet Entry GPS-RXD(Input)) |

| Class | Document | Message |
|---|---|---|
| Warning | main.SchDoc | Nets Wire TXD1 has multiple names (Sheet Entry GPS-RXD(Input),Net Label TXD1,Net Label TXD1) |
| Warning | ethernet.SchDoc | NetU7_12 contains IO Pin and Output Port objects (Port RXD1) |
| Warning | ethernet.SchDoc | NetU7_13 contains IO Pin and Output Port objects (Port RXD0) |
| Warning | ethernet.SchDoc | NetU7_15 contains IO Pin and Output Port objects (Port CRS_DV) |
| Warning | ethernet.SchDoc | NetU7_16 contains IO Pin and Output Port objects (Port REF_CLK) |
| Warning | ethernet.SchDoc | NetU7_17 contains IO Pin and Output Port objects (Port RXER) |
| Warning | ethernet.SchDoc | NetU7_18 contains IO Pin and Output Port objects (Port INT) |
| Warning | ethernet.SchDoc | NetU7_21 contains IO Pin and Input Port objects (Port TXD1) |
| Warning | main.SchDoc | Net U_TX has no driving source (Pin U1-42,Pin U4-4) |
| Warning | main.SchDoc | Unconnected Sheet Entry ETH-INT(Output) at 1020,140 |
| Warning | main.SchDoc | Unconnected Sheet Entry ETH-RXER(Output) at 1020,160 |