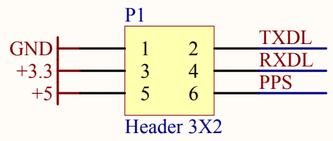
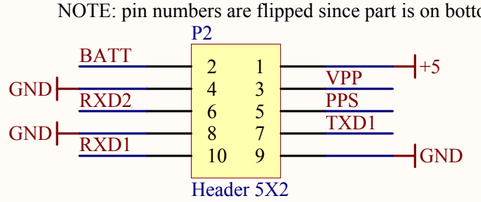
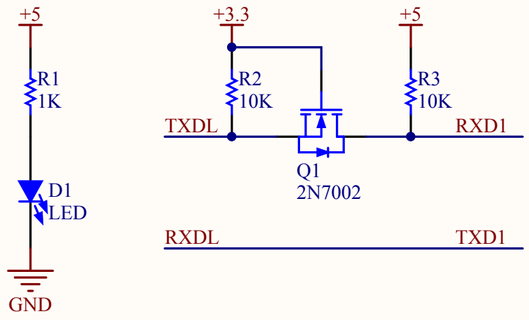


NOTE: pin numbers are flipped since part is on bottom





Title	*Adapter for Oncore GT+/UT+ Rcvrs*		
Size: A4	Number:*	Revision:1	
Date: 2012-12-02	Time: 17:53:40	Sheet of	
File: adapter_oncore.SchDoc			

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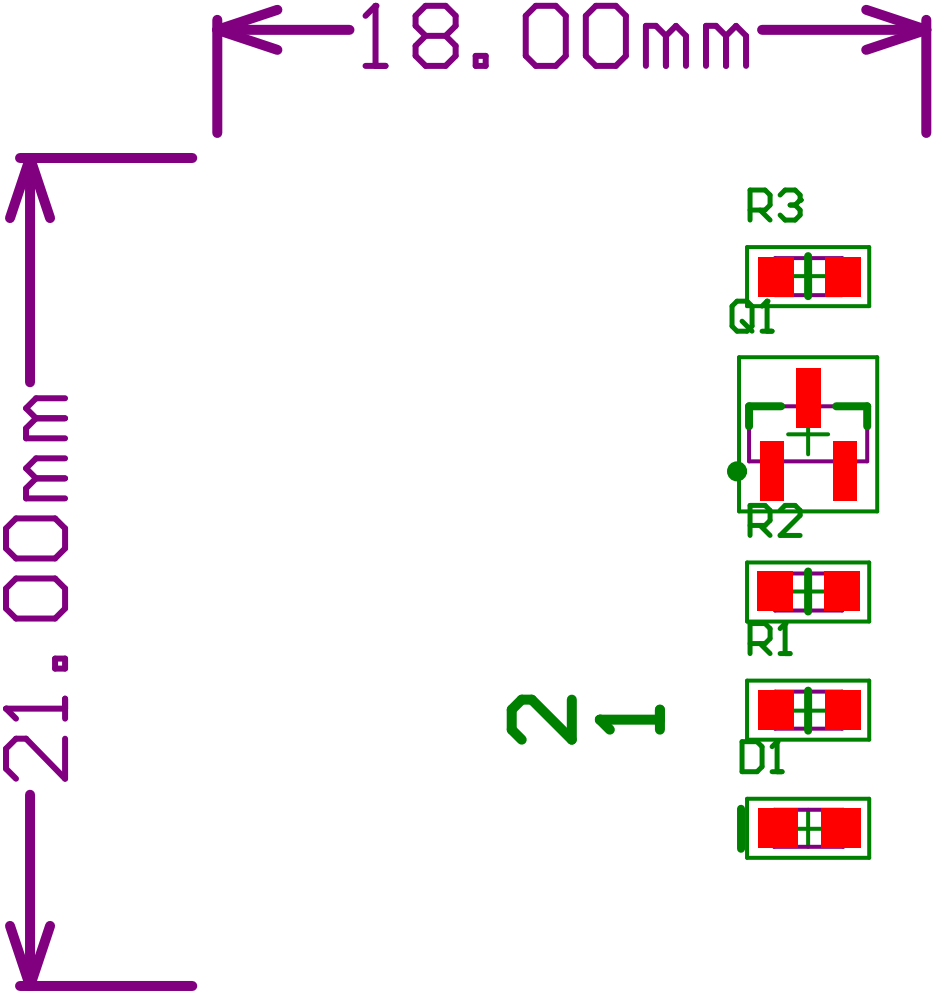
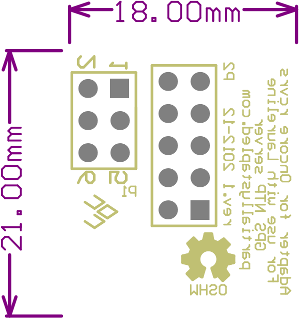

18.00mm
21.00mm
R3
Q1
R2
R1
D1
2
1


18.00mm
21.00mm

Design Rules Verification Report

Filename : D:\Users\RadiganConagher\Documents\circuits\laureline\adapter_oncore\adapter_oncore.PcbDoc

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Net Antennae (Tolerance=0mm) (All)	0
Silk to Silk (Clearance=0mm) (All),(All)	0
Silkscreen Over Component Pads (Clearance=0mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.076mm) (All),(All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Hole Size Constraint (Min=0.025mm) (Max=100mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Width Constraint (Min=0.254mm) (Max=0.254mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm)	0
Clearance Constraint (Gap=0.254mm) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Total	0

Electrical Rules Check Report

Class	Document	Message
Warning	adapter_oncore.SchDoc	Nets Wire RXDL has multiple names (Net Label RXDL,Net Label TXD1)